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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/026,118	12/21/2001	Darren L. Anand	FIS9-2001-0253-US1	4954

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INTERNATIONAL BUSINESS MACHINES CORPORATION  
DEPT. 18G  
BLDG. 300-482  
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HOPEWELL JUNCTION, NY 12533

EXAMINER

PHAM, LY D

ART UNIT

PAPER NUMBER

2818

DATE MAILED: 10/17/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

# Office Action Summary

Application No.

10/026,118

Applicant(s)

ANAND ET AL.

Examiner

Ly D Pham

Art Unit

2818

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

## Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

## Status

- 1) ☒ Responsive to communication(s) filed on 21 December 2001.
- 2a) ☐ This action is FINAL. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

## Disposition of Claims

- 4) ☒ Claim(s) 1-16 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-16 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

## Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 21 December 2001 is/are: a) ☐ accepted or b) ☒ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- 11) ☐ The proposed drawing correction filed on \_\_\_\_\_ is: a) ☐ approved b) ☐ disapproved by the Examiner.  
If approved, corrected drawings are required in reply to this Office action.
- 12) ☐ The oath or declaration is objected to by the Examiner.

## Priority under 35 U.S.C. §§ 119 and 120

- 13) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☐ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.
- 14) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).  
a) ☐ The translation of the foreign language provisional application has been received.
- 15) ☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

## Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892) 4) ☐ Interview Summary (PTO-413) Paper No(s). \_\_\_\_\_
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) 5) ☐ Notice of Informal Patent Application (PTO-152)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) \_\_\_\_\_ 6) ☐ Other: \_\_\_\_\_

### **DETAILED ACTION**

1. This office acknowledges receipt of the following items from the applicant:  
Information Disclosure Statement (IDS) was considered.
2. Claims 1 – 15 are presented for examination.

### ***Drawings***

3. Although fig. 1 of the drawings is fully labeled, the Office strongly suggest that fig. 1 be revised, for the sake of clarity, to additionally include the conventional naming label for all of the components as described in the specification instead of only the numerical labels. As an example, box 25 should add 'DRAM array'. If the boxes in the current figure are too small, it is recommended that they be sufficiently enlarged to enclose its name. For instance, boxes 30, 40, 110, etc.... Consequently, the figure can be made larger if necessary.

### ***Claim Rejections - 35 USC § 103***

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims 1, 4, 6 – 9, 12, and 14 – 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun (US Pat 6,128,704) in view of Dono et al. (US Pat Pub 2002/0015328 A1).

**Regarding claims 1 and 9**, Jun discloses a multibank DRAM macro (col. 2, lines 1 – 3), said macro comprising:

- (a) a plurality of DRAM memory banks, each bank respectively comprising:
  - (i) an array of DRAM memory cells (fig. 1, array 24 or 24'),
  - (ii) bitlines and wordlines, respectively defining columns and rows of the array (fig. 1, Y pipeline 25' and X pipeline 25),
  - (iii) a row address decoder circuit (fig. 1, X pipeline decoder),
  - (iv) a column address decoder circuit (fig. 1, Y pipeline decoder),
- (b) a bank select input for each respective bank, each bank input controlling operation of its respective bank (col. 2, lines 4 – 11), and
- (c) a data path receiver/driver shared by at least two banks (col. 3, lines 15 – 19).

Although Jun does not disclose the feature in which each bank comprises spare rows and columns, however, Dono et al. have shown this feature for redundancy purposes (paragraph 0002). Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to integrate the spare rows and columns feature to the disclosure of Jun to improve the yield to memory circuit, as reasoned by Dono et al.

**Regarding claims 4 and 12,** Dono et al. further shows the DRAM macro of claim 1, wherein said macro further comprises a write enable input (page 5, table 1, write enable WE)

**Regarding claims 6 and 14,** Dono also shows that each memory bank further comprises at least one sense amplifier (fig. 1, 15).

**Regarding claims 7 and 15,** it is considered a design choice as each bank of the DRAM macro has a capacity of about 1Mb of data.

Likewise for **claims 8 and 16**, Dono et al. show an exemplary DRAM macro, which comprises 4 of said banks (fig. 1, memory array SDRAM) as claimed in claims 7 and 15, respectively.

6. Claims 2 – 3 and 10 – 11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun and Dono et al. as applied to claim 1 above, and further in view of Yamaguchi (US Pat 6,067,632).

**Regarding claims 2 – 3 and 10 – 11**, although Jun and Dono et al. did not further disclose a multibank DRAM macro with a master select input, wherein the bank select inputs are latched to a falling edge of a signal from said master select input. Nevertheless, Yamaguchi has shown this feature in his invention (col. 13, lines 39 – 45). Therefore, it would have been obvious to one of ordinary skill in the art, at the time the invention was made, to include the claimed feature so that circuit size can be made small (col. 13, lines 46 – 57).

7. Claims 5 and 13 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun and Dono et al. as applied to claim 1 above, and further in view of Jeddeloh et al. (US Pat 6,430,742).

**Regarding claims 5 and 13**, although Jun and Dono et al. did not show the DRAM macro of claim 1 further comprises a page mode select input, Jeddeloh et al. however has illustrated this feature (col. 3, lines 8 – 19). Therefore, it would have been obvious to one of ordinary skill in the art, to combine the page mode feature to the DRAM structure of Jun and Dono so that fast memory transfer for a large segment of data can be obtained.

*Conclusion*

7. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

8. When responding to the office action, Applicant(s) are advised to provide the examiner with the page and line numbers in the application and/or references cited to assist the examiner to locate the appropriate paragraphs.

9. A shortened statutory period for response to this action is set to expire 3 (three) months and 0 (zero) day from the date of this letter. Failure to respond within the period for response will cause the application to become abandoned (see MPEP 710.02(b)).

10. Any inquiry concerning this communication on earlier communications from the examiner should be directed to Ly Pham, whose telephone number is 703-305-4862. The examiner can normally be reached on Monday – Friday from 8:30am to 5:00pm, alternate Friday off. The examiner's supervisor, David Nelms, can be reached at 703-308-4910. The fax number for the organization where this application or proceeding is assigned is 703-308-7724.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-308-0956.

Ly Pham



October 8, 2002



HOAI HO  
PRIMARY EXAMINER